

Attorney Docket No.: 00CON102P

REMARKS

In the Office Action dated May 18, 2004, the Examiner has *finally rejected* claims 1-9 and 11-28 pending in the application. Reconsideration and allowance of outstanding claims 1-9 and 11-28 in view of the following remarks are requested.

A. Rejection of Claims 1-3, 7-9, 21-23, and 27-28 under 35 USC §102(e)

The Examiner has rejected claims 1-3, 7-9, 21-23, and 27-28 under 35 USC §102(b) as being anticipated by U.S. Patent Number 5,574,939 to Keckler, et al. ("Keckler"). For the reasons discussed below, Applicants respectfully submit that the present invention, as defined by independent claims 1, 9, and 21, is patentably distinguishable over Keckler.

Embodiments according to the present invention relate to an apparatus and method for an improved performance VLIW processor. Conventional VLIW processors result in an advantage in parallel processing of a large number of instructions. However, conventional VLIW processors exhibit unnecessary power consumption while permitting the execution of only a single issue group per clock cycle. Additionally, conventional VLIW processors require a relatively large chip area and extra power for an instruction bus that wider than necessary. As an example, in a typical conventional VLIW processor, it would take four clock cycles to execute two VLIW packets each of which included two issue groups.

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In contrast, in embodiments according to the present invention, the two VLIW packets could be executed in only two clock cycles with little or no increase in consumed power. A reason for this achievement is that the present system accomplishes simultaneous execution of, for example, two independent issue groups belonging to different VLIW packets.

More specifically, referring to pages 19 and 20 and Figure 3 of the present application, one embodiment of the present invention utilizes two processing units, i.e., thread A processing unit 303 and thread B processing unit 305, as opposed to the single processing unit used in the conventional VLIW processors. The unique architecture and issue grouping of the present system results in a doubling of the execution speed of the VLIW process, in one embodiment, as discussed herein. However, this doubling of the execution speed does not result in a doubling of the consumed power or increased chip area, as described in the present application at, for example, pages 23 and 24. Consequently, the present system differs from prior attempts to increase the processing speed of VLIW processors.

Independent claim 1 recites language indicating that, in one embodiment, a plurality of threads each comprise one of a plurality of processing units. A plurality of instruction packets each comprise a plurality of issue groups. Each of the threads receive a respective issue group and execute the issue groups in a single clock cycle. Independent claims 9 and 21 recite similar limitations. Inherent in the independent claims is the idea

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of simultaneous execution of, for example, two independent issue groups belonging to different VLIW packets.

In contrast, Keckler discloses a plurality of processing units, wherein each processing unit comprises a synchronizer for selecting one of a plurality of threads of computation for execution in that unit. Although operations can be executed in parallel, Keckler does not teach simultaneous execution of two or more independent issue groups belonging to different VLIW packets. Therefore, Keckler does not disclose, teach, or suggest the present invention as defined by independent claims 1, 9, and 21, nor does Keckler achieve some of the advantages of the present invention discussed above. For example, Keckler does not achieve reduced power by using a smaller bus.

For the foregoing reasons, Applicants respectfully submit that the present invention as defined by independent claims 1, 9, and 23 is not taught, disclosed, or suggested by Keckler. Thus, independent claims 1, 9, and 23 are patentably distinguishable over Keckler. As such, the claims depending from amended independent claims 1, 9, and 23 are, *a fortiori*, also patentably distinguishable over Keckler for at least the reasons presented above and also for additional limitations contained in each dependent claim.

B. Rejection of Claims 4-6, 11-20, and 24-26 under 35 USC §103(a)

The Examiner has rejected claims 4-6, 11-20, and 24-26 under 35 USC §103(a) as being obvious with respect to Keckler in view of alleged "Applicants' admitted prior art."

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Applicants respectfully submit that claims 4-6, 11-20, and 24-26 depend from independent claims 1, 9, and 21, and thus, claims 4-6, 11-20, and 24-26 should be allowed at least for the same reasons discussed above in conjunction with patentability of independent claims 1, 9, and 21.

C. Conclusion

Based on the foregoing reasons, the present invention, as defined by independent claims 1, 9, and 21, and claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, outstanding claims 1-9 and 11-28 are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early Notice of Allowance directed to claims 1-9 and 11-28 pending in the present application is respectfully requested.

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Respectfully Submitted,
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